Design Rules for Microfluidic Soft Lithography at Caltech's Foundry

RGS 8/31/04

1. INTRODUCTION

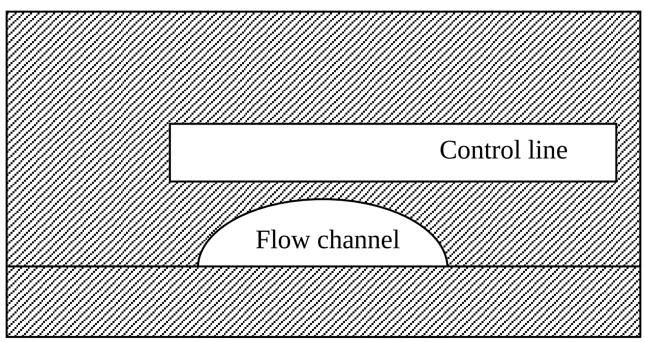
This document describes the basic design rules for microfluidic devices fabricated at the Caltech Microfluidic Soft Lithography Foundry. Following these rules for a design improves the chances that the devices will be easily manufactured and operational. This document assumes that the reader has an understanding of the basic Multilayer Soft Lithography fabrication process.

All the rules apply to devices made with both GE RTV 615 and Sylgard 184 silicone elastomers (poly(dimethylsiloxane) or PDMS). These elastomers are very similar to each other and no significant differences exist between devices made with them. The main differences between the two elastomers are in the chip fabrication protocols, not in the chip design, performance, or characteristics.

2. VALVE GEOMETRIES

A. Push-down valves

Configuration: Control lines pass over the flow channels. Pneumatic/hydraulic pressure in the control lines flattens down the flow structure creating a seal. This geometry is suitable only for low aspect ratio (1:10), shallow (approx 10µm) flow-structures and does not allow for deep reaction chambers to be integrated on the flow layer. This geometry is particularly well suited to applications were the flow structure must be in direct contact with the substrate (e.g. spotting DNA, patterned substrate, etc)



Standard Flow Geometry: Flow features before re-flow are 100 microns wide by 11 microns high. Rounded features have a maximum height of 13 microns. These features are molded from Shipley SPR-220-7.0 positive resist (requires a positive mask).

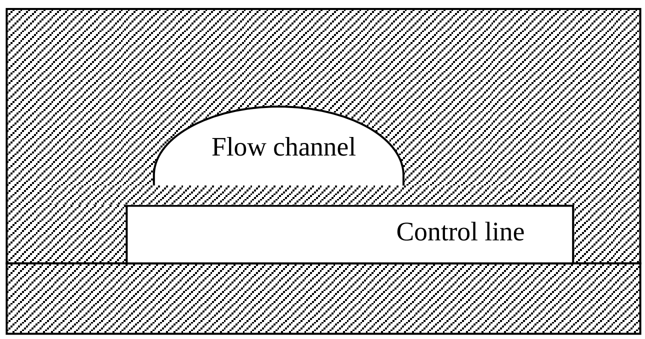
Standard Control Geometry: Control lines at valve junctions are 100µm wide (making a 100µm * 100µm valve area). Control line cross-overs (crossings between control lines and flow channels where no valve is desired) are 15 to 30µm wide. Control features are molded from either 10 to 12µm high SPR-220-7.0 resist (positive mask) or from 25µm high SU8-2025 resist (negative mask). For applications that require fast valve response the 25µm SU8-2025 features are preferred. SU8-2025 features cannot be closer than 40µm. For applications that require dense control structures (spacings as small as 15µm) the SPR-220-7.0 features are preferred.

Sealing to Substrate: The chip flow structures may be sealed either directly onto a glass cover-slip / glass slide, or by a third layer of PDMS. For PDMS sealed chips the sealing layer is 30µm of 20:1 GE RTV.

Devices sealed to glass are rated to 6psi flow pressures before delamination results. Devices sealed with a third layer of PDMS are rated to 20psi flow pressure. These large flow pressures are useful for high-performance devices where high actuation speeds are required (e.g. fast mixing applications). After sealing with the third layer of PDMS, the devices can be mounted on a glass slide, which might have a thin layer of PDMS spun on it to improve adhesion.

A. Push-up valves

Configuration: Control lines pass under the flow channels. Pneumatic pressurization of the control line causes a membrane to deflect up into the flow structure, sealing the channel. Deep reaction chambers may be integrated into the flow layer (upwards). Furthermore, high SU8 flow structures (without valves) may be included as low-impedance flow paths for high-speed applications. This is a better valve geometry than push-down, allowing for the closing of deep flow channels and for low actuation pressures.



Standard Flow Geometry:

a. Shallow Channel Option: The standard flow geometry suitable for most applications. Flow features before re-flow are 100 microns wide by 11 microns high. Rounded features have a maximum height of 13 microns. These features are molded from Shipley SPR-220-7.0 positive resist (require a positive mask).

b. Deep Channel Option: For applications that require suspensions of large particles (eukaryotic cells, large beads ...). Channels are fabricated from AZ 100 resist (positive mask). Rounded dimensions are 200 microns wide by 45 (+/- 3)µm high.

Standard Control Geometry:

a. Shallow Channel Option: Control lines at valve junctions are 100µm wide (making a 100µm * 100µm valve area). Control line cross-overs (crossings between control lines and flow channels where no valve is desired) are 15 to 30µm wide. Control features are molded from 25µm high SU8-2025 resist (negative mask). SU8-2025 features cannot be closer than 40 µm.

b. Deep Channel Option: Control lines at valve junctions are 200µm wide (making a 200µm * 200µm valve area). Control line cross-overs are 15 to 30µm wide. Control features are molded from 25µm high SU8-2025 resist (negative mask). SU8-2025 features cannot be closer than 40 µm.

Sealing to Substrate: The chip flow structures may be sealed either directly onto a glass cover-slip / glass slide, or by a third layer of PDMS. After sealing with the third layer of PDMS, the devices can be mounted on a glass slide, which might have a thin layer of PDMS spun on it to improve adhesion.

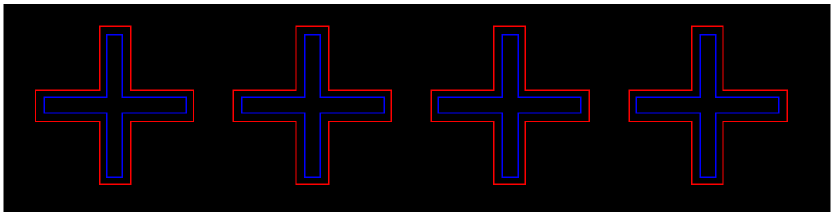
3. Basic Design Rules

1. No structure (control or flow) can be fabricated having an aspect ration lower than 1/10. The aspect ratio is defined as the quotient of the structure height to the minimum lateral dimension (height/width). Structures with lower aspect ratios are prone to collapse. If a feature is wider than this design rule permits, support posts must be added to ensure the aspect ratio is no lower then 1/10 in-between posts (i.e. posts every 100μm for a 10μm high structure).

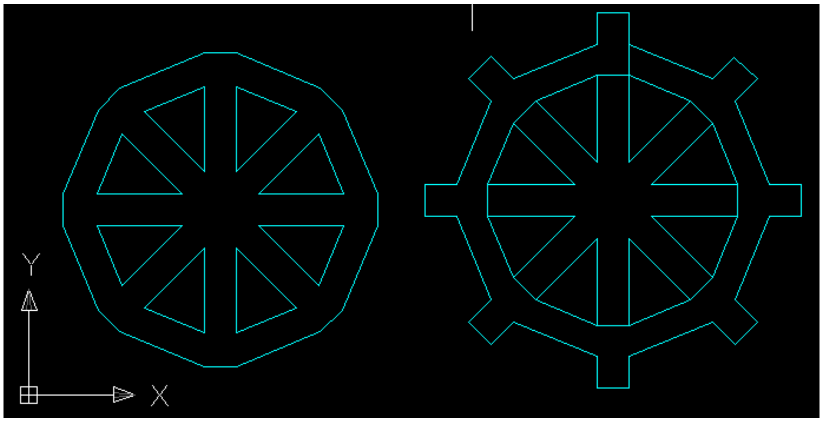
2. All devices must be designed with a border indicating where the chip should be diced.

3. If more then one chip is designed on a wafer there must be at least 2 mm spacing between the borders of adjacent devices.

4. All devices must have standard alignment marks (for aligning the different PDMS layers to each other). These should include marks near the most critical chip features, and marks at the periphery of the device (four corners). If possible a string of alignment marks along a chip edge is useful. The standard alignment mark is a cross as shown below. These marks are available in fluid architect or may be cut and pasted from the provided AutoCAD file (std-punch- align-marks.dwg).



5. Standard input/output holes are created with 20 gauge and 15 gauge punchers. Other sizes are available if required. All punch locations must be clearly marked with a standard punch marker. Standard punch markers are available in fluid architect. The standard 20 guage punch marker and 15 gauge punch marker for AutoCAD drawings is shown below. These markers have been designed to scatter light from all angles and facilitate visualization. These markers may be copied and pasted from the provided AutoCAD file (std-punch-align-marks.dwg).



6. Minimum center to center punch spacing for 20 guage I/O's is 1500 μm. Minimum center to center spacing for 15 guage I/O's is 2000 μm.

7. Designs must incorporate sufficient tolerances to allow for easy layer/layer registration. Designs must account for alignment tolerances of 30 μm. This means that the device must be designed to function properly despite 30 μm errors in alignment in all directions.